For Live Classes, Recorded bectures, Notes & Past Papers visit: www.megaleeture.com Made by. Muhammad Zohaib Credits to: Siz Jain Merchants, Barran Ahmed. Pictures from: Course Book, Siz Zain Notes. Von Neumann Model: Features of Von Neumann Model: > Central Processing Unit A placesson able to access memory directly -> Computer memories that could store programs as well as data. -> Stored programs made up of instructions that could be encuted in sequential order. Data Address bus bus MDR MAR PC Control Control CIR Unit bus Other registers Arithmetic and Logic Unit

<u>Components of the CPV:</u> -> <u>Avithmetric Logic Unit(ALU)</u>: Allows avithmetric or logic operations to be carried Out: youtube.com/c/MegaLecture/ The Accumulator (Acc) +9203367780041250515tes Used when carrying out For Live Classes, Recorded Lectures, Notes & Past Papers visit:

-> Control Unit (CV): The CU reads instructions from the memory, the instruction is then interpreted. Using this process signals are generated to tell the other components their jobs. The control Unit also ensures synchronization of data flow and program instructions throughout the computer.

-> System Clark: A system clock is used to produce timing signals on the control bus to ensue the synchronization that takes place.

-> Immediate Access STORE (IAS): The IAS holds all the data and the programs that the CPV needs to access. IAS is also known as the RAM of the computer, CIV can directly access the RAM and the RAM is considerably faster than Secondary storage.



¥ (5.8	Prediction	www.megalecture.comvert instruction that is	
~ ~ ~	jister (CIR)	being decoded and executed.	
At Inde	n Register (IR)	: Used when carrying out Inden addressing	
		Operations in Assembly Language.	
A Memor	y Address	: Stores the address of the memory	
Regis	y Address Her (MAR)	: Stores the address of the memory location currently being read from or	
•		written to.	
& Memo	my Data:	Stores data which has just been read	
	ster (MDR)	from memory or data which is just	
Ţ		about to be written to memory.	
		V	
* Prog	ian Counter	: Stores the address where the next	
CPC		instruction to be read can be found.	
# Stat	tws Register	: Contains bits which can be set or	
6	tws Register SR)	cleared according to operation.	
		0	
Sys	TEM BUSES:		
Su	pten buses are	used in computers as a popullel	
		onent; each with transmits one bit of	
	ta.		
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Address Bus: The Address Bus carries addresses throughout the computer system. The bus is unidirectional, meaning it travels in one direction only. The wider the bus the more addresses that can be transferred through the address bus.

2) Data Bus:

The Databus is bidirectional Callows data to be transferred in both directions.) The Databus transfers the data between components. The wider the bus the larger the word length that can be transported. youtube.com/c/MegaLecture/ +92 336 7801123

(3) (ontrol Bus: The control But is also bidirectional. It carries signals from the control unit to all the other components. Vsually 8-bits wide since only carries control signals. Components and their impacts on computer performance: () System Clock: ► The clock speed of a system determines the minimum time. interval between processing and enecution of consecutive instruction. ► By increasing the clockspeed and the clockcycles/frequency, we are able to process and enerute move instructions within the same period. ---- known as overdocking? ► As a result, the processing speed of the system increase, however, we cannot conclude that the Overall performance of the system improves solely based on this.

2) Address / Data Bus: ► AS mentioned previously, the width of the address bus and the databus are also important in deciding a computers performance, as they control how many addresses are youtube.com/c/MegaLecture/ directly accessible 92 338 78000 23000 bits of data can be

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(3) Cache Memory: ► Cache memory is similar to RAM in that it stores the currently required data and instructions. ► When a processor reads the memory, it first checks the cache memory and then the RAM. The benefit of using cache memory is that since it uses SRAM as compared to the DRAM that's used by RAM memory, it has a faster access time and can improve Computer performance. (4) Number of Coves: - Another way to improve computer performance is to increase the number of cores A single cove is mode up of a CU, an ALU and all standard registers. However, the increase in performance is not proportional. to the increase in number of cores. For enample, doubling the number of coves from 2 to 4 does not mean that the performance youtube.com/c/MegaLecture/ will+923367800123

→ This is because we need to consider the different cores Now having to communicate with each other as well (which takes time).
L In a dual core system reach core only needs to communicate with one other core, whereas in a quad core system, each core needs to communicate with 3 other cores, which takes up processing power and time.

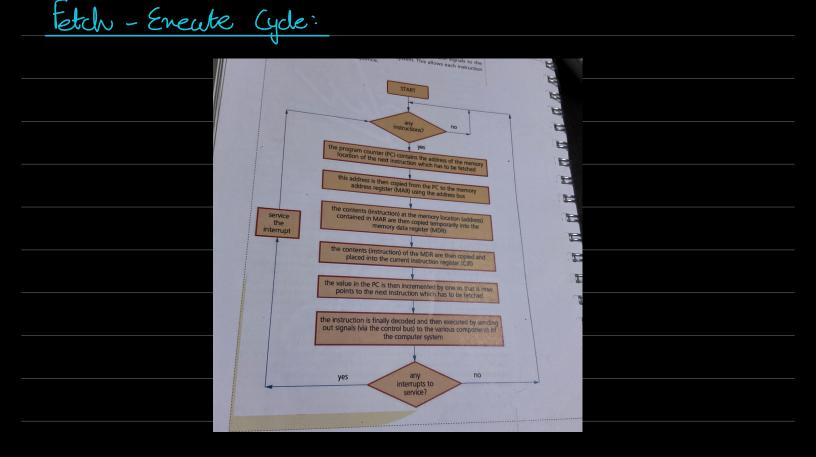
Computer Ports:

Input and Output devices are connected via ports. (1) USB Ports:

> Asynchronous serial data transmission method.
> Standard method of transferring data.
> USB cable consists of four-wired shielded cables, two wires for power and earth and two for data transmission.

Pros of USB Cons of USB -> Devices plugged into the computer -> The manimum cable length are automatically detected and is approximately 5m. device drivers are automatically loaded up. > Never USB standards are youtube.com/c/MegaLecture/

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	event transmission	
rates Support	ted.	
, , ,		
High - Definition	on Multimedia Interface	CHOMI)
v	AND	
	Video Grap	thics Array (VGA)
Type of Cable	Pros	Cons
Type of Cable (1) HDMI	-> The current standard for	\Rightarrow Not a very robust connection.
	Modern screens.	
	-> Allows for a very fast	-> Limited cable length to
	data transfez rate	retain signal strength.
	-> Improved security	-> There are multiple
	-> Supports modern digital	connection standards.
	Systems.	
23 VG A	-> Only one standard	-> Outdated analogue
	available	technology
	-> It is easy to split the	-> The cable must be of
	connection	high grade to ensure good
		Undistorted signal
		-> It is very easy to
		bend the pins when connecting ture/
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Register Transfer Notation:

(1)MAR [PC7 of PC copied to MAR. Contents [PC] + 1 PC PC is incremented by 1. (2)3 [[MAR]] MDR Data stored at address shown in MAR is copied into MDR /4) CIR [MDR] Contents of MDR copied into the CIR. Double brackets are used in line 3 because it is not MAR contents

being copied into the MDR but it is the data stored at the address Stoved in the MAR.

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Interrupts:

An interrupt is a signal sent from a device or from Software to the processor. This causes the processor to temporcrily Stop what it is doing and service the interrupt.

How interrupts are handled dwing the fetch enecute cycle: At the end of the fetch enecute cycle the processor checks for interrupts. The computer is checked for an interrupt flog. The processor identifies the source of interrupt and then checks for the priority of the interrupt. If the interrupt priority is above the current task, then processor saves the contents of the current registers and calls the interrupt handles that services the interrupts when the service is complete the contents of the registers are restored, and processor continues with fetch enecute.